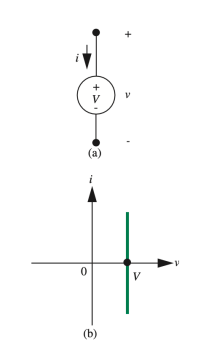
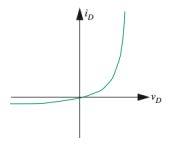
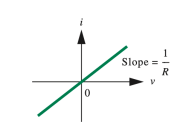
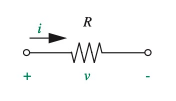
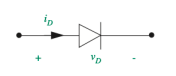
Three terminal devices 

• Two terminal devices have fixed IV characteristics



• Three terminal devices – IV of two terminals can be controlled using the third terminal.

• Examples – Switch (linear), Transistors (non-linear)

Switch – IV Characteristics

• IV characteristics between terminal �! and �" is controlled by � �

�! �"

�� = ”1” (��)

� = ”0” � = ”1” **Switch OFF Switch ON**

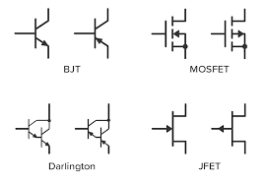
� = ”0” (���) �

Switch – Types

• Depending on the control, the switch can be

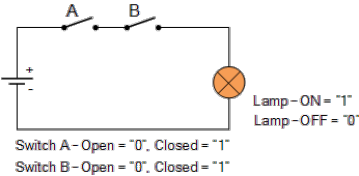
• **Analog**: Controlled using physical toggle/button

• **Digital**: Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)

**Analog switches Digital switches (Transistors)**

Switch Application – Logic Gates • We can use switches to build logic gates

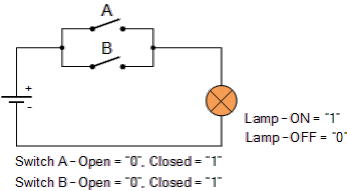
**A B Bulb**

**0 0 0 1 1 0** 

**OFF OFF OFF**

**AND operation**

**1 1 ON A B Bulb**

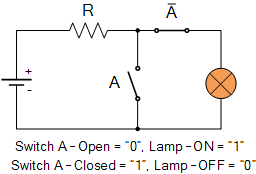
**0 0 0 1 1 0** 

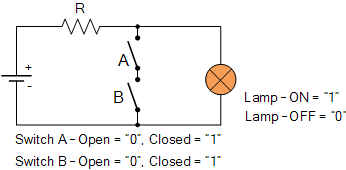
**OFF ON ON**

**OR operation**

**1 1 ON**

Switch Application – Logic Gates

**A Bulb**

**A B Bulb**

**A B Bulb**

**0 1**

**ON OFF**

**0 0 0 1 1 0**

**ON ON ON**

**0 0 0 1 1 0**

**ON OFF OFF**

**NOT operation**

**1 1 OFF NAND operation**

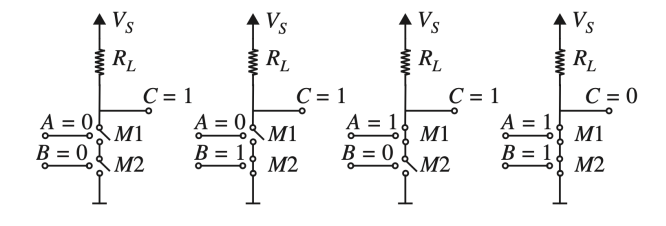
**1 1 OFF NOR operation**

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits -> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

Switch Application – Logic Gates Alternative representations:

Switch Application – Logic Gates

Alternative representations:

*Vss Vss Vss Vss*

Switch Application – Logic Gates

� ���� 0 5V 1 0V

� � ���� 0 0 5V 0 1 5V 1 0 5V 1 1 0V

� � ���� 0 0 5V 0 1 0V 1 0 0V 1 1 0V

Examples

Example

Implement using switches: � = (� + �)�

Digital Representation

• Binary → Two states (0/False, 1/True)

• Binary variables in circuit, need to use two states of device/parameters **Voltage Current State**

5V 🡪 1 0V 🡪 0

0V 🡪 1 3.3V 🡪 0

2mA 🡪 1 3mA 🡪 0

ON 🡪 1

OFF 🡪 0

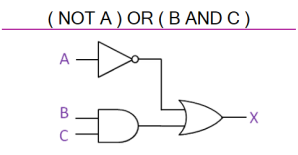
Low resistance 🡪 1 High resistance 🡪 0

Digital Representation

Suppose you want to send 010110

• Single value based representaion fails in the presence of noise • Better approach – threshold-based system

• Simplest: Logical 0 = � < �# Logical 1 = � > �#

Static Discipline 

• Specification for digital devices

• Requires devices to adhere to common representation to ensure that **valid input produces valid output**

• This means, if

• Sender sends “0” Receiver interprets as “0” • Sender sends ”1” Receiver interprets as “1”

Static Discipline

Naïve approach: Single threshold based system 5V

�$ = 2.5 �

1

Valid 1

1

sender

Logical 0: �% < �$

receiver

Logical 0: �& < �$

sender 2.5V receiver

Logical 1: �% > �$

Logical 1: �& > �$

0

0V

Valid 0

0

What if �& = 2.5�? Undefined!

Static Discipline Double threshold based system 5V

�' = High voltage threshold = 3� �( = Low voltage threshold = 2�

1

3V

Valid 1

Forbidden

1

sender

Logical 0: �% < �( Logical 1: �% > �'

receiver

Logical 0: �& < �( Logical 1: �& > �'

sender receiver Region

2V

0

0V

Valid 0

0

What if �%= 1.9� and channel noise is 0.5�?

�& = 1.9� + 0.5� = 2.4� = invalid

🡺 valid output producing invalid input,

i.e., no margin for noise

Static Discipline

Four threshold based system 🡪 Tighter restriction on sender (**output**) �)' = Output high voltage threshold = 4.5�

1

5V

4.5V 3V

Valid 1 NM1

�)( = Output low voltage threshold = 0.5�

�\*' = Input high voltage threshold = 3�

1

�\*( = Input low voltage threshold = 2�

Forbidden

sender receiver Region

sender

receiver

2V

NM0

Logical 0: �% < �)(

Logical 0: �& < �\*(

0.5V 0

Logical 1: �% > �)'

Logical 1: �& > �\*'

0

0V

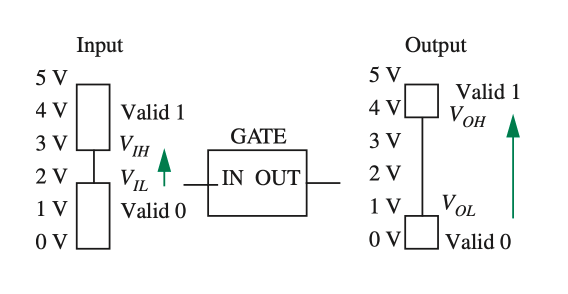
Valid 0

For static discipline, �)( < �\*( < �\*' < �)'

Noise margins (NM):

• ��+ = �)' − �\*' = 4.5 − 3 = 1.5� (signiJicance? ) • ��, = �\*( − �)( = 2 − 0.5 = 1.5� (signiJicance? )

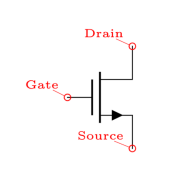
Static Discipline

Four threshold based system 🡪 Tighter restriction on sender (**output**)

Transistors as Digital Switch

• Transistors are 3 terminal non-linear devices, can be used as switch • 2 types – Voltage Controlled, Current Controlled

• **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET) are voltage controlled • Control, � = �!". The IV characteristics (�#" �� �#") depends on �!" • Actual dependency is complex.

• Will start with a simple (but approximate) one – **S-Model** (Switch Model) 

MOSFET S-Model

• The MOSFET (approximately) behaves like a switch • � = �$%. Here, � = “0” ⇒ �$% < �#, and � = “1” ⇒ �$% ≥ �#

MOSFET S-Model



Logic Gates using MOSFET Just replace the switches with MOSFETs!

*Vss Vss Vss*

NOT Gate (Inverter) NAND Gate (Inverter) NOR Gate (Inverter)

MOSFET Logic Gates – More Examples

*Vss Vss Vss*

��� = �� + � + � ��� = � + � �� = � + � ��

Voltage Transfer Characteristics (VTC)

• Reminder: VTC is a graph where x axis = input voltage, y axis = output voltate • Why? Design logic gates to follow a given static discipline

When �\*- < �$ Logical 0 , �).$ = �/ = 5� (Logical 1)

When �\*- ≥ �$ Logical 1 , �).$ = 0 (Logical 0) *Vss*

VTC of NAND gate

• We only have one x axis, but two inputs

• Solution: Draw two VTC, one considering �Y = 0, one considering �Y = 1 A = "0" A = "1"

*Vss* A = "0" A = "1" When �0 = 0 When �0 = 1 

*Vss Vss Vss Vss*

VTC of NAND gate

• We only have one x axis, but two inputs

• Solution: Draw two VTC, one considering �Y = 0, one considering �Y = 1 A = "0" A = "1"

*Vss* A = "0" A = "1"

When �0 = 0 When �0 = 1

**Homework:** Find VTC for NOR gate

Construction of Real MOSFET

100 

��

Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100 μm. (Photograph Courtesy of Maxim Integrated Products.)

Construction of Real MOSFET

Simplified cross section 

and 3D view

No channel, open ckt �12 = 0� �12 > �$



Channel created Will have some R -> SR model

SR Model



�)- =1

�45 �~~�~~ (�12 − �$)=1

��)6

Unit of � = ��/�7

• SR model is a better approximation than S model

• However, still an approximation. This model fails when �32 increases to around �12 − �$

SR Model - Inverter

*Vss*

For example, if �2 = 5�,

�)- = 1 �Ω, �( = 14 �Ω *Vss Vss Vss Vss* 

*Vss*

�).$,'&9: = �2 �).$,(%; = �2�)-

*Vss Vss*

�)- + �(≠ 0

Design of logic gates Expected

�

�� � ���

*Vss*

**Low (�!" < �#) High (5�) Low (�$%# = �$%#,'()) High (�!" < �#) Low (�$%#,'()) High (5V)

Actual

�� � ���

Low (�!" < �#) High (5�) Low (�$%# = �$%#,'()) High (�!" < �#) Low (�$%#,'() = 0.5 �) Low (�$%# = �$%#,'()

�$ = 0.4 �, �2 = 5�, �)- = 1 �Ω, �( = 9 �Ω

*Vss*

�).$,'&9: = �2 = 5� �).$,(%; = �2�)-

�)- + �(= 51

1 + 9= 0.5 �

Therefore, need to design logic gates properly such that



*Vss Vss Vss*

Design of logic gates - Example

Assume the following values for the inverter circuit parameters: �! = 5 �, �" = 1 �, and �� = 10 �Ω. Assume, further, that #

$\*+ %,-= 5 for the MOSFET. Determine a &' sizing for the MOSFET so

that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter. **Solution:**

�2�)-

�)- + �(< �$

⇒ 5�)-

�)- + 10 < 1

⇒ 5�)- < �)- + 10 ⇒ �)- <104= 2.5

Now, �)- =1

�45 �~~�~~ �)6= 5×1

�/�

�/� < 2.5 ⇒�� >52.5 Hence 5

⇒�� > 2

Review – MOSFET

Control = �!" = �! − �", controls the IV between drain-source (�#" vs �#")

Threshold voltage = �$, minimum voltage required to create the channel

**Models**

**1. S Mode**: Assumes an ideal channel with zero resistance

**2. SR Model**: Assumes finite channel resistance, �%&, depends on �!" − �$ = �%'

MOSFET Linear Models

S Model SR Model



�!" =1

�#$ �~~�~~ (�%& − �')=1

��!(

Real MOSFET

• Why �%& =2

3!" #$ ('%&4'')=2

3'()? Because channel width ∝ �%', and � ∝2

56789

• For small �#", uniform channel, hence fixed �%&, therefore SR model valid. • As �#" is increased, channel becomes tapered cause �!# ↓. Resistance ↑, slope ↓. • This mode is called the **triode mode**. Condition: �#" < �%'



Real MOSFET

• When �#" = �%', channel pinches off.

• Increasing �#" further have no effect on channel shape. Hence, current saturates • This mode is called the **saturation mode**. Condition: �#" ≥ �%'

• Behaves like a **current source** (constant current) that depends on �%'

IV Characteristics of Real MOSFET

**Mode Condition Equation** 

Cutoff �%& < �' �) = 0

�)& < �!(�) = �[�!(�)& − 12 �)&\* ]

Triode �%& ≥ �'

�)& ≥ �!(�) =�2 �!(

Saturation �%& ≥ �'

\*

�!( = �%& − �'

� = �#$��

Solving Circuits with MOSFET

• Use **Method of Assumed State**!

• Three steps:

• **Assume**: One of the modes (Cutoff, Triode, Saturation) • **Solve**: Use corresponding equation and KCL+KVL

• **Verify**: Check if the conditions of �!" and �#" are satisfied. If not, repeat.

• Might need to solve quadratic equation (��$ + �� + � = 0).

• If we get two roots, choose the one that’s *favorable* to your assumption

Example 1



The MOSFET is specified as �! = 1� and � = 0.5 ��/�". Find �# and �$ for �% = 2�.

**Solution:**

Step 1: Assume the MOSFET in **saturation**

Step 2: �) =�2 �!(

\* Here, �%& = �% − �& = �% − 0 = �% = �+ = 2� Therefore, �!( = �%& − �' = 2 − 1 = 1�

∴ �) =0.52 1 \* = 0.25 ��

Again, �)& = �) − �& = �) − 0 = �) = �-

KVL along �,: �)×1�Ω + �- = 5 − 0 ⇒ �. = 5 − �)×1�Ω ⇒ �- = 5 − 0.25×1 = 4.75 � = �)&

Step 3: �%& = 2� �)& = 1�

> �' > �!(

Therefore, **assumption correct**!

√

√

Correct ans: �) = 0.25 ��, �-= 4.75 �

Example 2



The MOSFET is specified as �! = 1� and � = 0.5 ��/�". Find �# and �$ for �% = 5�.

**Solution:**

Step 1: Assume the MOSFET in **saturation**

Step 2: �) =�2 �!(

\* Here, �%& = �% − �& = �% − 0 = �% = �+ = 5� Therefore, �!( = �%& − �' = 5 − 1 = 4�

∴ �) =0.52 4 \* = 4 ��

Again, �)& = �) − �& = �) − 0 = �) = �-

KVL along �,: �)×1�Ω + �- = 5 − 0 ⇒ �. = 5 − �)×1�Ω ⇒ �- = 5 − 4×1 = 1 � = �)&

Step 3: �%& = 5� �)& = 1�

> �' ≯ �!(

√ ×

Therefore, **assumption wrong**!

Example 2



The MOSFET is specified as �! = 1� and � = 0.5 ��/�". Find �# and �$ for �% = 5�.

**Repeat:**

Step 1: Assume the MOSFET in **triode**

Step 2: �) = �[�!(�)& − 12 �)&\* ]

Here, �%& = �% − �& = �% − 0 = �% = �+ = 5�

Therefore, �!( = �%& − �' = 5 − 1 = 4�

Again, �)& = �) − �& = �) − 0 = �) = �-. Assuming �)& = � KVL along �,: �)×1�Ω + �-= 5 − 0 ⇒ �) =/0(!"

,= 5 − �

∴ �) = 0.5 4×�)& − 12 �)&\* ⇒ 5 − � = 0.5 4� − 12 �\* ⇒ 5 − � = 2� − 0.25�\* ⇒ 0.25�\* − 3� + 5 = 0

Solving, � = 2�, � = 10� Since �)& = � is small in triode, smaller value of � is favorable

Therfore, �- = �)& = � = 2�, and �) = 5 − � = 3 ��

Step 3: �%& = 5� �)& = 2�

> �' < �!(

√ √

Therefore, **assumption correct**! Correct ans: �) = 3 ��, �-= 2 �

Example 3 

Step 2: �) =�2 �-1\*

Let's assume �. = �& = �

Here, �%& = �% − �& = �% − �- = 2 − �

Therefore, �!( = �%& − �' = 2 − � − 1 = 1 − �

Again, �)& = �) − �& = �) − �. = 5 − �

Ohm’s law for the resistor: �) =(#0.

,23= �

∴ � =42 1 − � \* ⇒ � = 2 1 − 2� + �\* ⇒ � = 2 − 4� + 2�\* ⇒ 2�\* − 5� + 2 = 0

The MOSFET is specified as �! = 1� and � = 4 ��/�".

Solving, � = 0.5, � = 2�

Since �)& = 5 − � is large in saturationsmaller value of � is favorable

Find �# and �$ **Solution:**

∴ �!= �" = � = 0.5�,�# = � = 0.5 ��,

�#" = 5 − � = 4.5�, �$" = 2 − � = 1.5�, and �%& = 1 − � = 0.5�

Step 1: Assume the MOSFET in **saturation**

Step 3: �%& = 1.5� �)& = 4.5�

> �' > �!(

√

√

Therefore, **assumption correct**! Correct ans: �) = 0.5 ��, �- = 0.5 �

Practice

**Hint Explanation** Assume �) = �. For 5�Ω: �) =,.0(!

/⇒ V4 = 10 − 5×�) = 10 − 5�.

For 3�Ω: �) =("0.

5⇒ V6 = 3×�) = 3�.

Therefore, V%& = �% − �& = 5 − 3�, and �!( = �%& − �' = 5 − 3� − 1 Also, V)& = �) − �& = 10 − 5� − 3� = 10 − 8�

Now if you assume saturation: �) =�2 �!(

\* ⇒ � =22 4 − 3� \*

And if you assume triode:

�) = �[�!(�)& − 12 �)&\* ]

⇒ � = 2[ 4 − 3� 10 − 8� − 0.5× 10 − 8� !] Solve for �, take the \_\_\_\_\_\_ root